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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,615	01/04/2002	Robert F. Wallace	SDK1P007/SDK0296.000US	2529

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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,615	WALLACE, ROBERT F.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5,6 and 12-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6 and 12-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The finality of the rejection of the last Office action is withdrawn in view of the present Office action.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,399,421 to Han et al.

Regarding claim 1, Han et al. (figure 3) teach a molded semiconductor device package comprising:

a die attach pad (59);

a first (42) and second (50) semiconductor die, each die having a die bond pad (48, 58), each of the die positioned such that the die bond pads (48, 58) of each die face in opposite directions, the first (42) and second (50) die being connected to opposing surfaces of the die attach pad (59);

a plurality of contact leads (62) positioned proximate to the first (42) and second (50) die;

a first bonding wire (40) that is stitch bonded to the die bond pad (48) of the first die (42) and stitch bonded to a first one of the contact leads;

a second bonding wire (40) that is stitch bonded to the die bond pad (58) of the second die (50) and stitch bonded to a second one of the contact leads; and

a molding cap (66) that encapsulates the first (42) and second (50) die, the first and second bonding wire (40), and a portion of the contact leads (62).

Han et al. differ from the claimed invention by not showing the molding cap has a thickness of less than about 1 millimeter. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the molding cap has a thickness of less than about 1 millimeter because it reduces the thickness of the device. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 5, Han et al. teach the first and second bonding wire (40) are formed of a material selected form gold (column 4, lines 41-42).

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,399,421 to Han et al. in view of US Patent No. 5,735,030 to Orcutt.

Regarding claim 2, the disclosures of Han et al. are discussed as applied to claims 1 and 5 above.

Han et al. differ from the claimed invention by not showing a first conductive ball formation that is formed between the first bonding wire and the die bond pad of the first die; and a second conductive ball formation that is formed between the second bonding wire and the die bond pad of the second die. However, Orcutt (figure 3) teaches a conductive ball formation (21) that is formed between the bonding wire (1) and the die bond pad (5) of the die (7). It would

have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Orcutt into the device taught by Han et al. because it is desirable securely to hold the wire on the chip. The combined device shows a first conductive ball formation that is formed between the first bonding wire and the die bond pad of the first die; and a second conductive ball formation that is formed between the second bonding wire and the die bond pad of the second die.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,399,421 to Han et al. in view of US Patent No. 6,437,429 to Su et al.

Regarding claim 6, the disclosures of Han et al. are discussed as applied to claims 1 and 5 above.

Han et al. differ from the claimed invention by not showing the package is either a thin small outline package or a quad flat pack package. However, Su et al. teach the package is a thin small outline package or a quad flat pack package (column 1, lines 13-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Su et al. into the device taught by Han et al., since it is a conventional semiconductor device package.

5. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,399,421 to Han et al. in view of US Patent No. 5,735,030 to Orcutt.

Regarding claim 12, Han et al. (figures 1-3) teach a molded semiconductor device package comprising:

a pair of semiconductor dice (42, 50) that are oriented such that a top surface of each die are facing in opposite directions, the top surface of each die having at least one die bond pad (48, 58);

at least one contact lead (62) positioned proximate to the pair of semiconductor dice (42, 50);

a molding cap (66) that encapsulated the pair of semiconductor dice (42, 50), the bonding wire (40) and a portion of the contact lead (62).

Han et al. differ from the claimed invention by not showing a conductive ball formation positioned on the die bond pad of each die and at least one bonding wire that is stitch bonded to the contact lead and stitch bonded to one of the conductive ball formations on the die bond pad. However, Orcutt (figure 1) teaches a conductive ball (21) formation that is formed on the die pad (5) and the bonding wire (1) is also stitch bonded to the contact lead (9) and stitch bonded to the conductive ball formation (21) on the die bond pad (5). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Orcutt into the device taught by Han et al. because it is desirable securely to hold the wire on the chip and the lead. The combined device shows a conductive ball formation positioned on the die bond pad of each die and at least one bonding wire that is stitch bonded to the contact lead and stitch bonded to one of the conductive ball formations on the die bond pad.

Regarding claim 13, Han et al. teach a die attach pad (59) that is attached to and sandwiched between the pair of semiconductor dice (42, 50).

Regarding claim 14, Han et al. teach the bonding wire (40) is gold. (column 4, lines 41-42).

Regarding claim 15, Han et al. differ from the claimed invention by not showing the molding cap has a thickness of less than about 1 millimeter. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the molding cap has a thickness of less than about 1 millimeter because it reduces the thickness of the device. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

6. Claims 16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,399,421 to Han et al. in view of US Patent No. 6,031,216 to Singh et al.

Regarding claim 16, Han et al. (figure 3) teach a molded semiconductor device package comprising:

a die attach pad (59);

a first (42) and a second (50) semiconductor die, each die having a die bond pad (48, 58), each of the die positioned such that the die bond pads of each die face in opposite directions, the first (42) and second (50) die being connected to opposing surfaces of the die attach pad (59);

a contact lead (62) positioned proximate to the first (42) and second (50) die;

a first bonding wire (40) that is stitch bonded to the contact lead (62) and stitch bonded to the die bond pad (48) of the first die (42), wherein the first bonding wire (40) was stitch bonded to the contact lead (62) after being stitch bonded to the die bond pad (48);

a second bonding wire (40) that is stitch bonded to the contact lead (62) and stitch bonded to the die bond pad (58) of the second (50) die, wherein the second bonding wire (40) was stitch bonded to the contact lead (62) after being stitch bonded to the die bond pad (58); and

a molding cap (66) that encapsulated the first (42) and second (50) die, the first and second bonding wire (40), and a portion of the contact lead (62).

The claim limitations "the first aluminum bonding wire was stitch bonded to the contact lead before being stitch bonded to the die bond pad and the second aluminum bonding wire was stitch bonded to the contact lead before being stitch bonded to the die bond pad" in claim 16 are taken to be product by process limitations which do not carry weight in claim drawn to structure. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al., 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly In re Thorpe, 277 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Han et al. differ from the claimed invention b not showing the aluminum wire. However, Singh et al. teaches the aluminum wire (column 1, lines 35-47). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Singh et al. into the device taught by Han et al. because it provides interconnection between the chip and the leadframe. The combined device shows the aluminum bonding wire.

Regarding claim 18, Han et al. and Singh et al. differ from the claimed invention by not showing the molding cap has a thickness of less than about 1 millimeter. It would have been

obvious to one having ordinary skill in the art at the time the invention was made for the molding cap has a thickness of less than about 1 millimeter because it reduces the thickness of the device. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 19, Han et al. teach the first die contains integrated circuit components configured to form a memory or a logic unit (column 1, lines 26-29).

7. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Han et al. in view of Singh et al., and further in view of US Patent No. 6,437,429 to Su et al.

Regarding claim 17, the disclosures of Han et al. and Singh et al. are discussed as applied to claims 16 and 19 above.

Han et al. and Singh et al. differ from the claimed invention by not showing the package is either a thin small outline package or a quad flat pack package. However, Su et al. teach the package is a thin small outline package or a quad flat pack package (column 1, lines 13-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Su et al. into the device taught by Han et al. and Singh et al., since it is a conventional semiconductor device package.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
April 5, 2004

Primary Examiner
Steven Loke